

Reinvigorating EDA in the Social Media Era

**Patrick Groeneveld
Synopsis**

Pittsburgh, March 2013

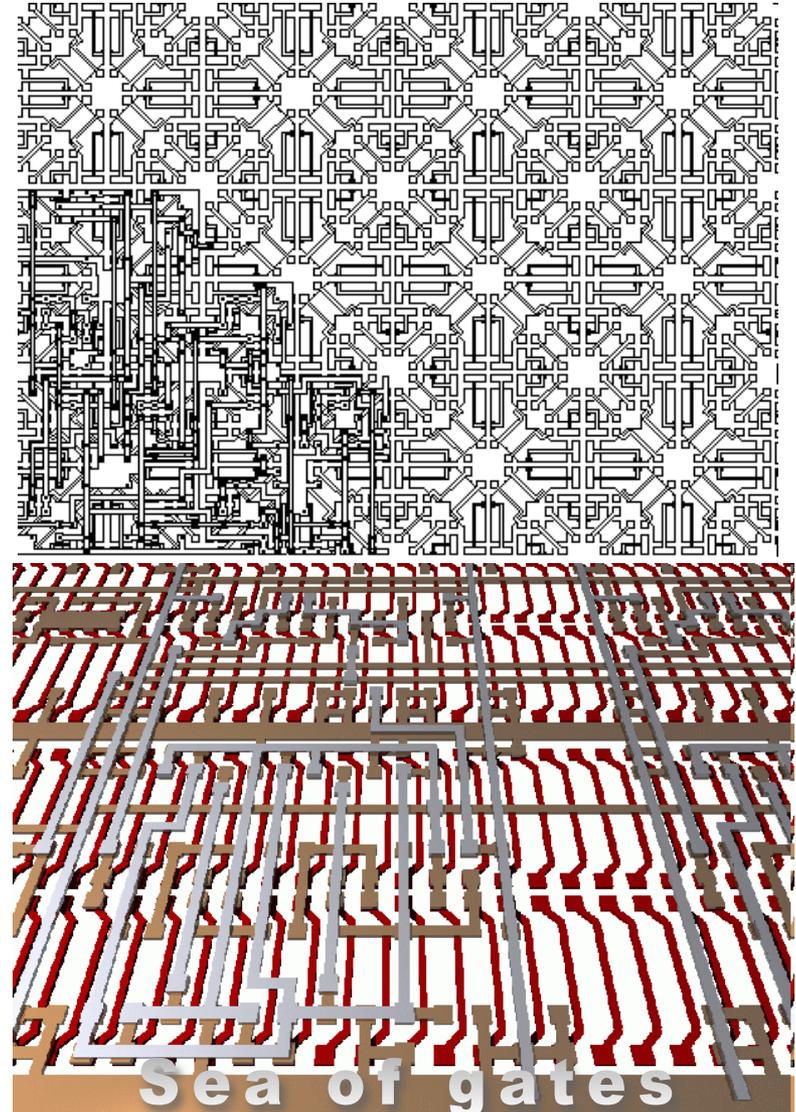
Summary

- **My history in Academic and Corporate EDA**
- **The current ‘state of the EDA’**
 - Dollars & People
 - Conferences
- **Solved and Unsolved problems**
- **Role of academia**

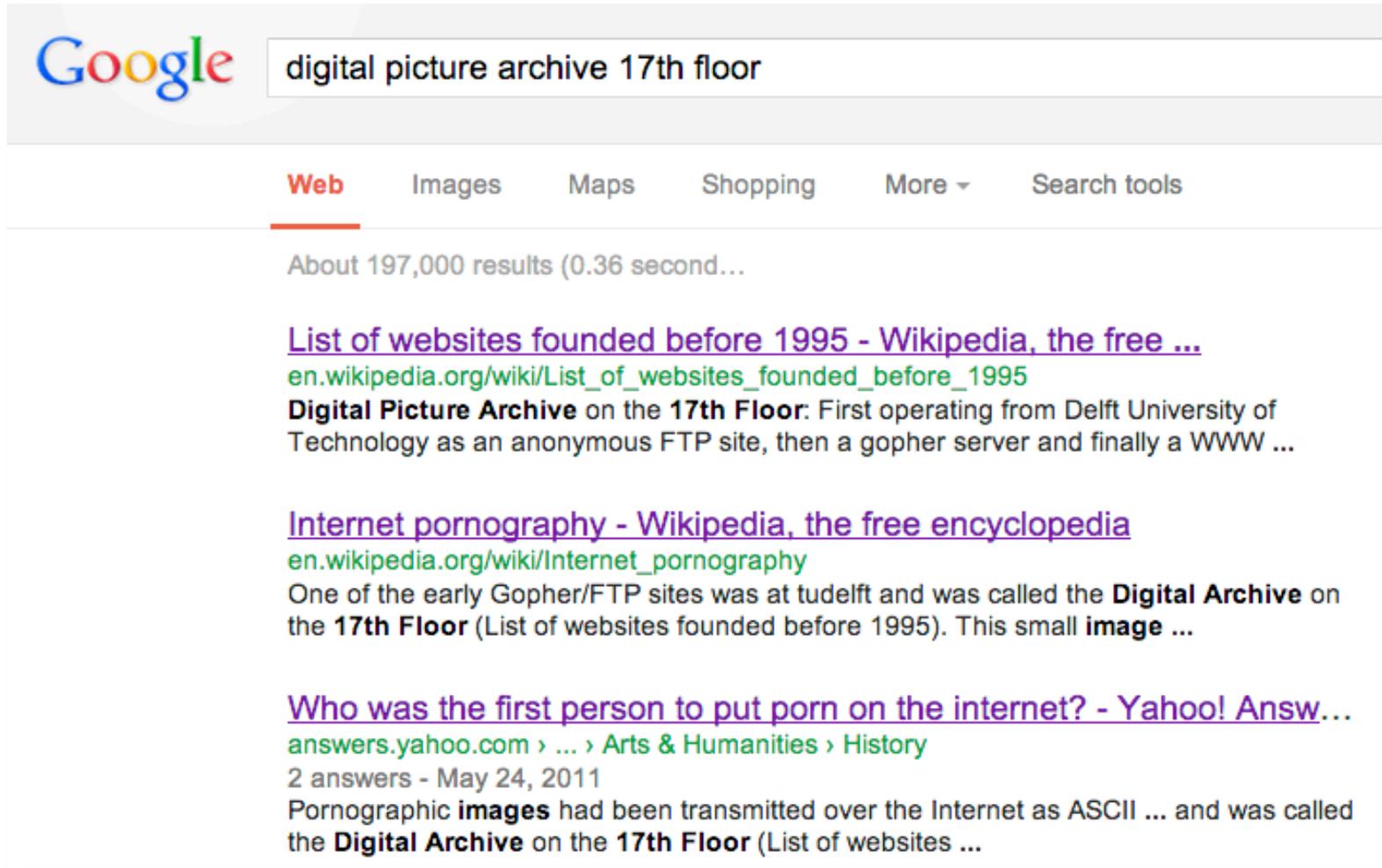
My EDA story, abridged

Can we replicate this for the current generation?

- **Delft University: Routing as MSc and PhD projects**
 - Sold it to National Semiconductor, Philips, Sagantec and Cadence.
- **Post doc @ Delft: Developed 'Ocean'**
 - For university system/IC design lab, 1991-today
 - Logic to a real Sea-of-Gates chip
- **Compass**
 - Datapath synthesis
- **Magma**
 - All aspects of Physical Synthesis
- **Full professor**
 - @ Eindhoven University
- **Magma again**
- **Synopsys**



University life: My 5 minutes of fame...



The screenshot shows a Google search interface. The search bar contains the text "digital picture archive 17th floor". Below the search bar, there are tabs for "Web", "Images", "Maps", "Shopping", "More", and "Search tools". The "Web" tab is selected. The search results show "About 197,000 results (0.36 second...)". The first result is a Wikipedia page titled "List of websites founded before 1995 - Wikipedia, the free ...". The second result is a Wikipedia page titled "Internet pornography - Wikipedia, the free encyclopedia". The third result is a Yahoo! Answers page titled "Who was the first person to put porn on the internet? - Yahoo! Answ...".

Google

digital picture archive 17th floor

Web Images Maps Shopping More Search tools

About 197,000 results (0.36 second...)

[List of websites founded before 1995 - Wikipedia, the free ...](#)
en.wikipedia.org/wiki/List_of_websites_founded_before_1995
Digital Picture Archive on the **17th Floor**: First operating from Delft University of Technology as an anonymous FTP site, then a gopher server and finally a WWW ...

[Internet pornography - Wikipedia, the free encyclopedia](#)
en.wikipedia.org/wiki/Internet_pornography
One of the early Gopher/FTP sites was at tudelft and was called the **Digital Archive** on the **17th Floor** (List of websites founded before 1995). This small **image** ...

[Who was the first person to put porn on the internet? - Yahoo! Answ...](#)
answers.yahoo.com > ... > [Arts & Humanities](#) > [History](#)
2 answers - May 24, 2011
Pornographic **images** had been transmitted over the Internet as ASCII ... and was called the **Digital Archive** on the **17th Floor** (List of websites ...

Switch to the Commercial world

Magma, August 1997



EDA industry: a management summary

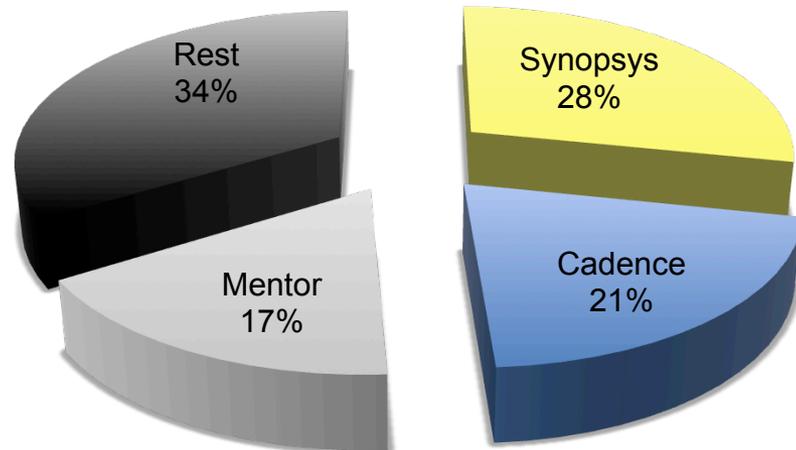
- **Dominated by 3 large companies:**

- Synopsys: 9000 people, Value \$5.29B, Revenue \$1.81B
- Cadence: 5600 people, Value \$4.03B, Revenue \$1.33B
- Mentor: 4400 people, Value \$1.93B, Revenue \$1.09B
 - (Jasper: 100 people, Value \$0.3B(?), Revenue <\$0.1B)

- **Total:**

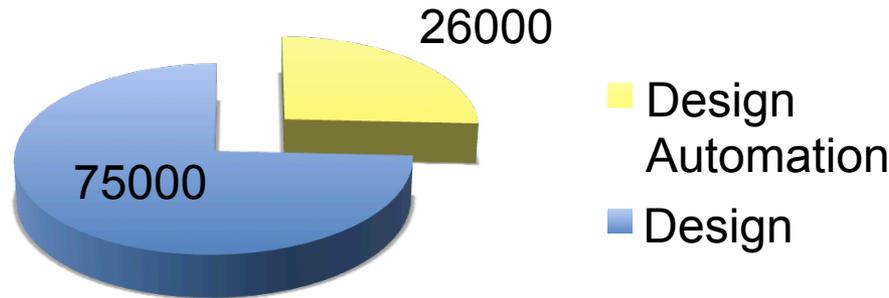
- About 26000 people
 - 30% R&D
- \$6.4B/year
 - \$4.8B core EDA

EDA industry revenue market share

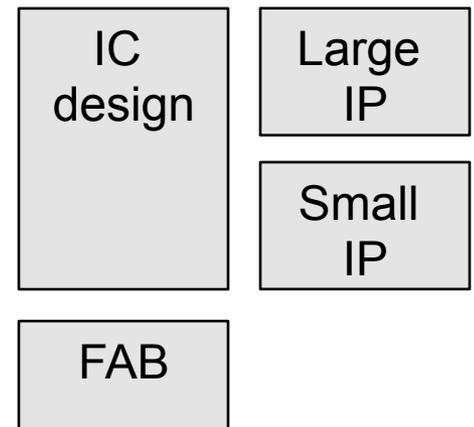


Perspective: is EDA right-sized?

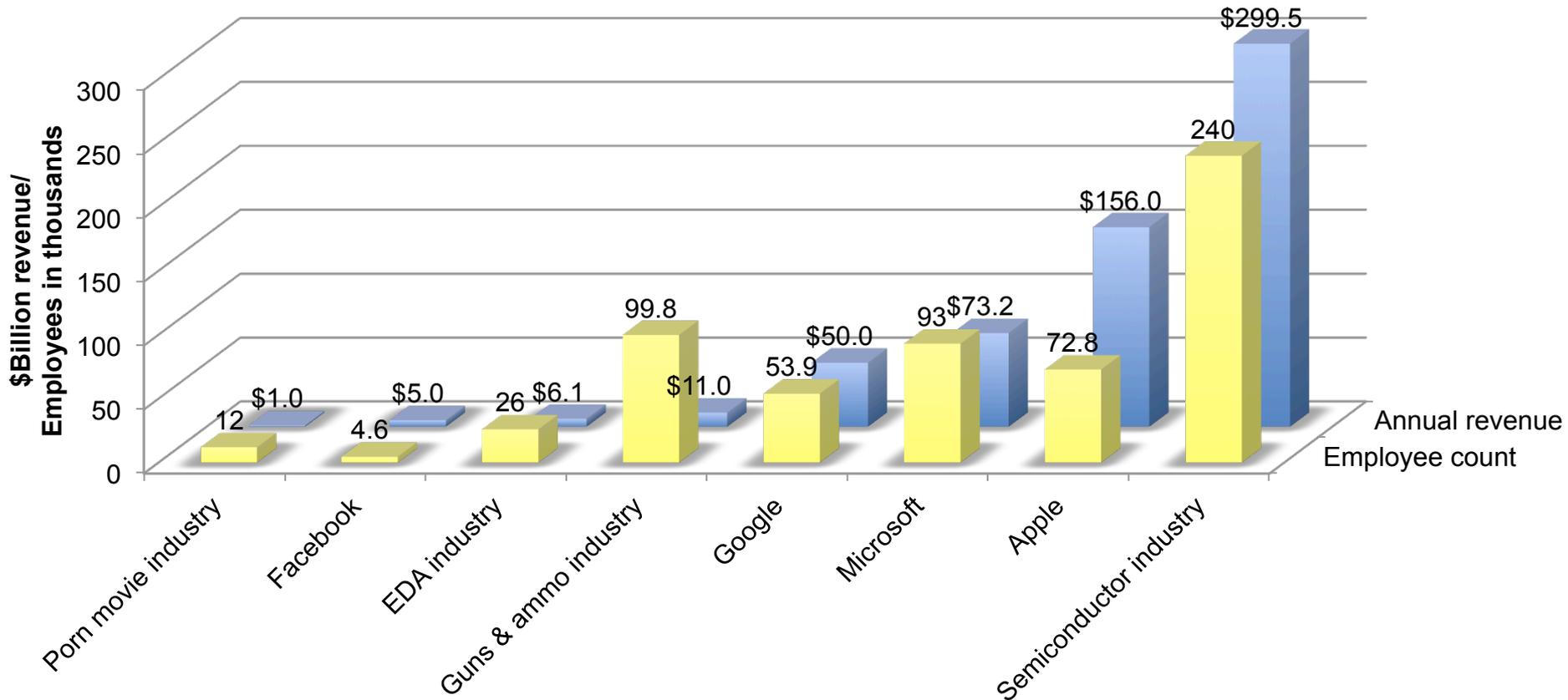
People in IC design



- **Steady decline of IC design starts**
 - But designs are radically more complex
- **Number of customers:**
 - Approx. 200 world-wide
 - But only 10 large ones
 - Trend: consolidation

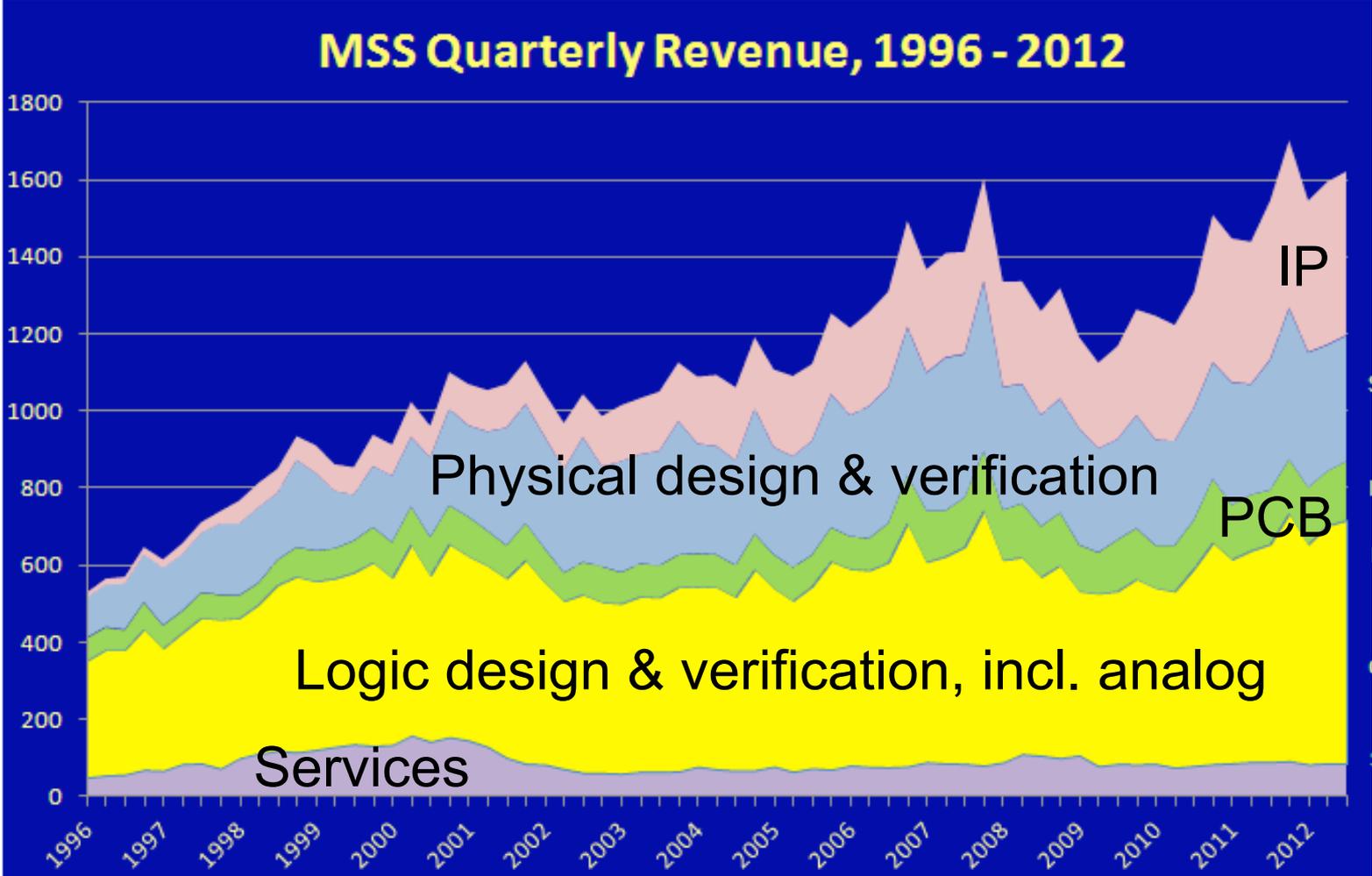


EDA Revenue: a perspective



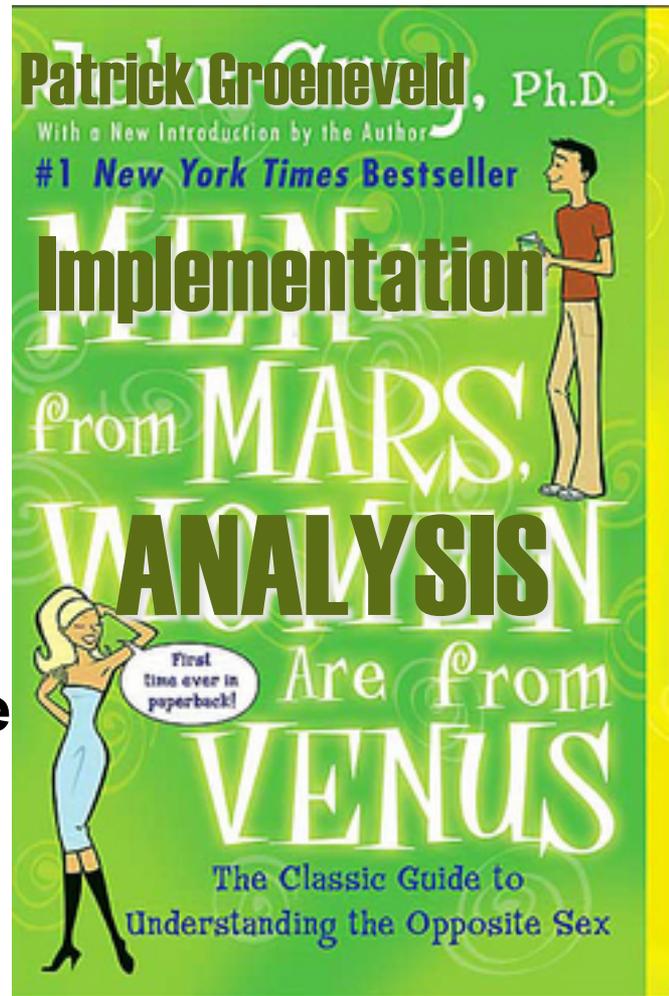
Sources: EDAC, National Shooting Sports foundation, yahoo finance, lamatreasure.com, wikipedia

Slow EDA growth, moderate IP growth



Implementation is from Mars, Analysis is from Venus

- Sign-off tools:
- Verification, extraction, STA, spice, DRC, LVS
- Highly accurate
- Big and slow
- Is the 'whiner'



- Implementation tools:
- RTL synthesis, Placement, Routing, Optimization, Humans
- Poor accuracy
- Lean, mean
- Is the 'hacker'

Need to make this work

What makes money in EDA?

- **Most is sold as ‘time-based license’**
 - Package deal for all tools
 - Very few ‘Pay per Use’

- **“I need more licenses, pronto!”**
 - Happens only for sign-off tools (DRC, timing, spice)

- **Sign-off tools make disproportionate amount**
 - Synthesis is a tougher sell
 - ... because tools are sold per CPU hour

DAC Conference perspective: the numbers

- **Exhibition:**

- Number of companies: steady at 200
 - But its more small companies, very few mid-side and 3 giants.
- Square footage: declining over past decade
 - Big-3 EDA are 70% of EDA revenue, but only 12% of DAC revenue!

- **Conference:**

- Attendees: 1400 = Steady after decline since 9/11
 - All-time high was in 3500 in 2000
- Papers: steady for many years (between 600-700)
- Added Designer Track: target non-scientific crowd

- **Overall attendance:**

- 2012: approx. 7200
 - All-time high was in 18000 in 2000

DAC Facebook page

DESIGN AUTOMATION CONFERENCE

JUNE 2 - 6, 2013
AUSTIN, TX



Design Automation Conference

3,250 likes · 664 talking about this · 0 were here

✓ Liked * ▾

Convention Center · Engineering Service · Educational |
Welcome to the new Design Automation Conference: the premier Electronic Design Automation and Embedded Systems & Software event. DAC brings

About Photos Likes Map Events

Highlights ▾

Status Photo / Video Offer, Event +

Write something...

 Design Automation Conference shared a link. February 13

What was the first year you attended DAC?

42 Friends Like Design Automation Conference



+33

Recommendations

Now

January

2012

2011

2010

2009

2008

2007

2006

2005

2004

2003

2002

2001

2000

1990s

1980s

1970s

1960s

Founded

See Your Ad Here

Design Automation Conference



Welcome to the new Design Automation Conference: the premier Electronic Design Automation and Embedd...

Like · Patrick Groeneveld likes this.

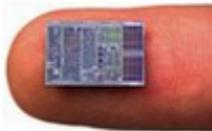
Advertise Your Page

Name	Status	Reach	Freq.	Social Reach	Actions
<input type="checkbox"/> Likes Cadence - Ad	▶ ▼	3,933	20.5	523	119

Ad Preview [Edit](#)

Targeting [Edit](#)

50th DAC celebration



Join the 50th Design Automation Conference + Cadence is 25 years at DAC.

You like Design Automation Conference.

- This ad targets 3,440 users:**
- who live in one of the countries: United States, India, Ireland, Italy, Japan, Armenia, Netherlands, Canada, South Korea, Spain, Sweden, United Kingdom, Israel, Finland, Denmark, Belgium, Australia, Austria, Russia, Brazil, China, Taiwan, France or Germany
 - age 18 and older
 - who like #Cadence Design Systems

[View on Site](#) - [Create a Similar Ad](#)

Close

<input type="checkbox"/> Likes Synopsys - Ad	▶ ▼	2,572	27.6	496	70
<input type="checkbox"/> Likes Mentor - Ad	▶ ▼	5,286	6.6	456	45
<input type="checkbox"/> Works at Synopsys - Sponsored Stories	▶ ▼	186	7.5	183	21
<input type="checkbox"/> Works at Mentor - Ad	▶ ▼	450	24.7	290	7
<input type="checkbox"/> Likes Synopsys - Sponsored Stories	▶ ▼	664	13.1	648	6
<input type="checkbox"/> Work at EDA companies - Sponsored Stories	▶ ▼	532	8.5	519	5
<input type="checkbox"/> Attend DAC through the Newton Young Student Fellow Program - Ad	▶ ▼	545	20.7	0	2
<input type="checkbox"/> Likes Mentor - Sponsored Stories	▶ ▼	310	7.5	307	1
<input type="checkbox"/> Work at EDA companies	▶ ▼	259	7.4	67	1
<input type="checkbox"/> Works at SemiconductorCompanies	▶ ▼	2,276	12.5	153	1
<input type="checkbox"/> Works at SemiconductorCompanies- Sponsored Stories	▶ ▼	442	4.2	414	1
<input type="checkbox"/> Attend DAC through the Newton Young Student Fellow Program - Sponsored Stories	▶ ▼	5	2.2	5	0

Who likes DAC?



Design Automation Confe... Timeline ▾

✓ Liked

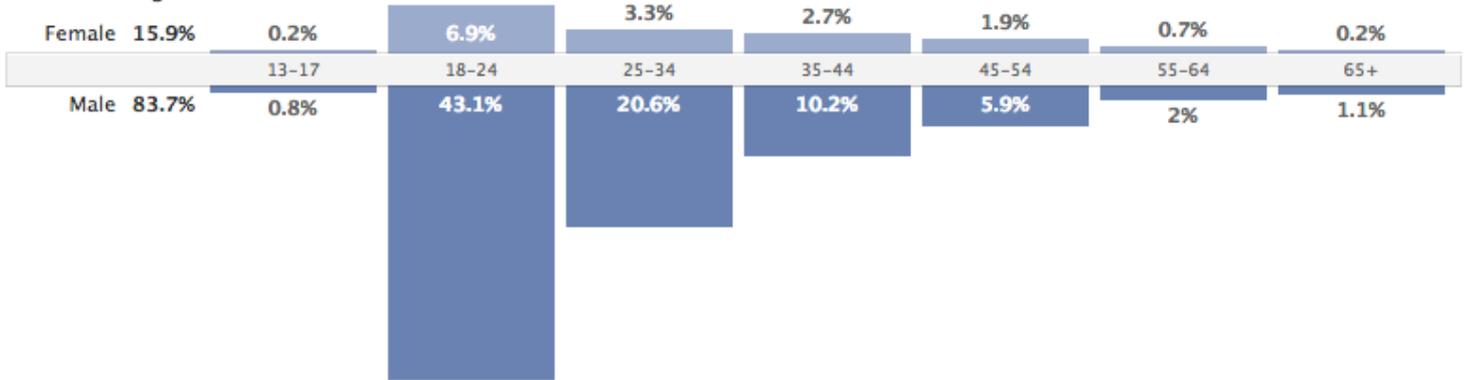
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 Export Data
  ▾

People Who Like Your Page (Demographics and Location)
[See Likes](#)

Gender and Age?



Countries?

- 1,521 India
- 613 Brazil
- 207 Taiwan
- 169 United States of America
- 144 Italy
- 101 Armenia
- 49 France

Cities?

- 134 Bangalore, Karnataka, India
- 98 New Delhi, Delhi, India
- 81 Taipei, Taiwan
- 81 Yerevan, Armenia
- 74 Hyderabad, Andhra Pradesh, India
- 58 Calcutta, West Bengal, India
- 43 Indore, Madhya Pradesh, India

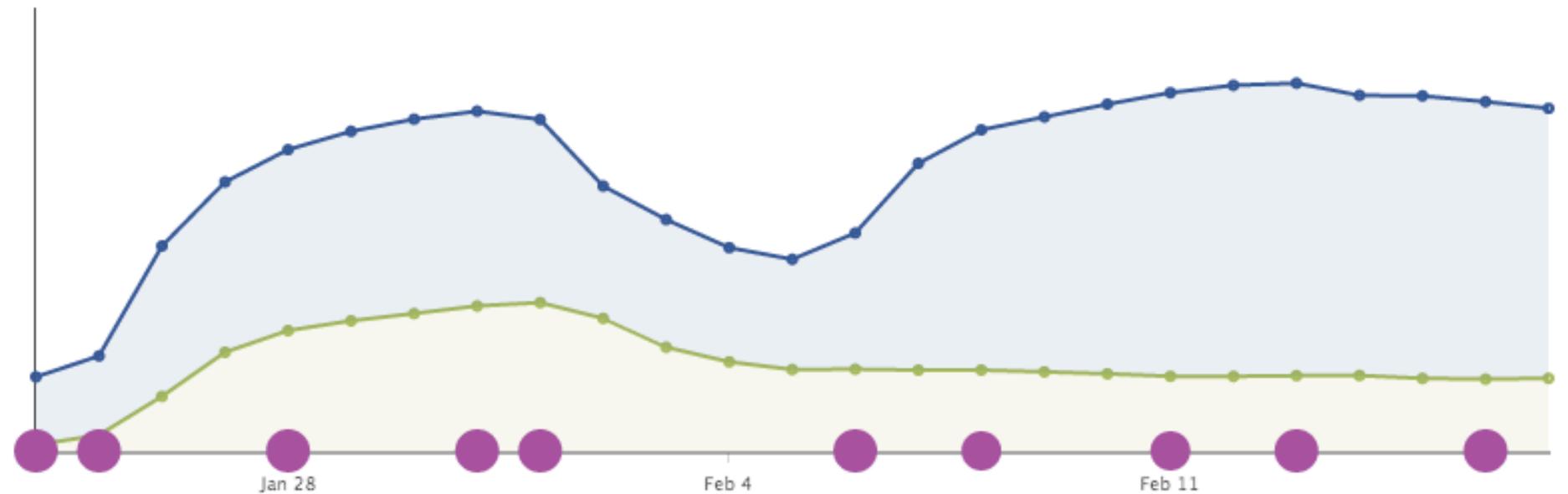
Languages?

- 1,751 English (US)
- 599 Portuguese (Brazil)
- 217 English (UK)
- 184 Traditional Chinese (Taiwan)
- 126 Italian
- 55 French (France)
- 41 Russian

3250 likes

Total Likes[?] **3,250** ↑ 15.99% Friends of Fans[?] **1,246,311** ↑ 16.06% People Talking About This[?] **640** ↓ -9.48% Weekly Total Reach[?] **110,101** ↓ -1.61%

Posts[?] People Talking About This[?] Weekly Total Reach[?]



Page Posts (Updated 4 minutes ago)

Observations: EDA business ecosystem

- **Trend 1: Consolidation**
- **Trend 2: Large EDA run their own shows**
 - Control message, do not want to share with competition
- **Trend 3: Outsourcing**
 - More design work is done in India
- **Japan & Europe are in decline**
 - Major companies losing the Semiconductor battle
- **Korea, China and India on the rise.**
- **Trend 4: Base EDA is 'commoditized'**
- **Embedded systems != EDA**

Observations: EDA Academia and conference

- **Paper flow steady**

- Though fewer active research groups
- Ivy league universities are less active in EDA
- More from Taiwan, Korea, China
- Less from Europe, USA and Japan

- **Paper quality steady**

- Though less exiting than a decade ago

- **Slowly more Embedded Systems papers**

- **Major EDA employees are MIA**

- Hardly ANY attendees from Synopsys, Cadence or Mentor at the major conferences!!!!

More observations: academic view

- **Weak empirical academic standards:**
 - Too few test cases
 - Test cases based on artificial data or flows
 - Many opportunities for **bias**

- **Reluctance to publish ‘negative results’**
 - Publication pressure encourages intellectual dishonesty
 - Comparisons/field tests are rare (or poor at best)

So, what is the role of academia?

- **1: Educating the next generation of engineers**
- **2: Research into radical new methods**

- **Challenge 1:**
 - Engineering is between ‘art’ and ‘science’
 - Often misunderstood by colleagues in ‘pure’ sciences
- **Challenge 2:**
 - Maintaining academic depth while being practically relevant
 - Find proper level of abstraction:
 - Not too high = useless in practice
 - Not too low = no academic depth
- **Challenge 3: (northern America and Europe)**
 - Attracting EDA students (by inspiring them)

Two-fold Design Complexity Increase

- **System complexity:**

Dealing with the sheer size of the system

- 10 Billion transistors, 500M+ gates

Exponential

- **Silicon complexity:**

Dealing with the physics of manufacturing technology

- Electrical parasitics.
- Leakage & dynamic power
- Process variability & manufacturing

More design iterations

Design Effort for a graphics chip family

Design Start	Technology node	Transistor count	Complexity	Front-end staff	Back-end staff
1993	0.5 μ	0.75M	1x	1.0x	1.0x
1995	0.5 μ	1.25M	1.5x	1.2x	3.0x
1996	0.35 μ	4.0M	4x	1.6x	3.0x
1997	0.31 μ	7.5M	7x	1.7x	4.0x
1998	0.25 μ	9.0M	10x	1.5x	4.0x
1998	0.22 μ	22M	20x	2.5x	5.0x
1999	0.18 μ	25M	22x	1.5x	4.0x
1999	0.15 μ	57M	30x	3.5x	6.0x
2000	0.15 μ	60M	35x	1.5x	7.0x
2000	0.15 μ	63M	40x	3.0x	7.0x
2001	0.13 μ	120M	50x	5.0x	9.0x

Physical Design of Apple processors

- **Common technology:**

- 45nm Samsung

- **A4: 2010**

- iPhone 4 & iPad 1
- 7.3mm x 7.3mm

- **A5: 2011**

- iPhone 4S & iPad 2
- 10.0mm x 10.0mm

- **A5x: 2012**

- iPad 3
- 12.9mm x 12.7mm
= 3x as big as the A4



Why is EDA so spectacularly successful in automatic design?

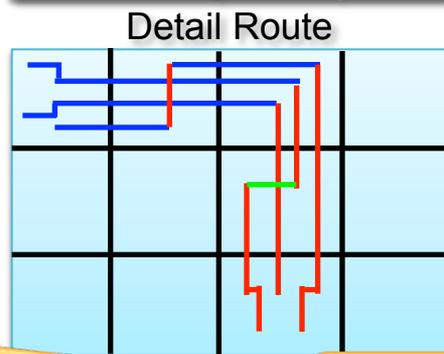
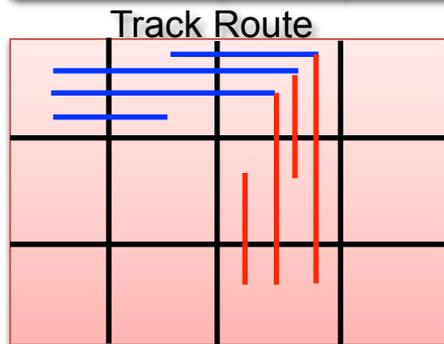
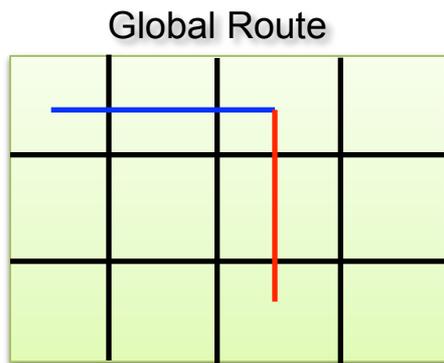
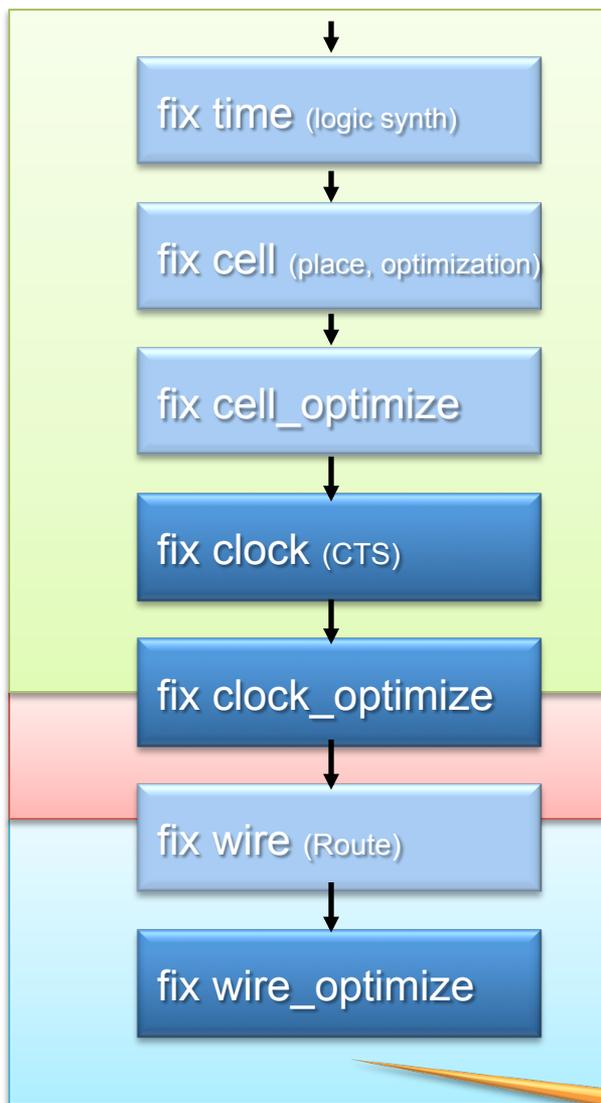
- **Unmatched when compared to any other industry:**
 - Synthesize billions of components
 - Designer productivity improvement follow exponential Moore's law for decades!
- **My view:**
 - Abstraction levels that *work*: RTL, net list, mask
 - A flow methodology that works without too much waste
 - A hierarchical decomposition that works
 - Agnostic for (most) applications
- **Recipe for success:**
 - Problem contained in a box (standard cell, macro)
 - Boxes are 'composable' using simple rules:
 - swap., Don't overlap, minimize wire length, and you're good
 - Simple model of reality is good enough for automatic optimization
 - 'Smooth' solution space

EDA handles *Many* Objectives Simultaneously

- **Correct & manufacturable mask pattern**
 - Congestion control
 - Big chip = good
- **Meets timing & electrical requirements**
 - Battle parasitics: timing, voltage drop
 - Big gates = good, compact chip = good & a little bit of a pain
- **Low power**
 - Leakage control, multi-voltage, sleep, etc
 - Small gates = good, complex floorplan = necessary evil
- **Low part cost**
 - Compact chip, dense wires = good
- **Low design effort**
 - Robust design, short tool run times, re-use
 - Simple = good, pushbutton = good

Intricate trade-off

Magma Flow: guided by 'best available' data



- Global route:
 - Layer assignment
 - Congestion
 - Resource contention
 - Detours
- Track route:
 - Refines global route
- Detail route
 - Copies track route
 - Fixes opens
 - Ripup & Reroute

The only thing that matters is the quality at the end!

Layout Design at different levels of abstraction

The image displays a multi-level abstraction of layout design in a CAD environment. The top window shows Verilog code for a divider circuit. Below it, a Schematic view shows the hierarchical structure of the divider units. The bottom section shows two different Layout views: a high-level abstract layout with a highlighted yellow path, and a detailed physical layout showing routing and timing analysis.

```
170. divide_count <= 0;
171. // dividend placed initially so that remainder bits are zero...
172. grand_dividend <= dividend_i << R_PP;
173. // divisor placed initially for a 1 bit overlap with dividend...
174. // But adjust it back by S_PP, to account for bits that are known
175. // to be leading zeros in the quotient.
176. grand_divisor <= divisor_i << (N_PP+R_PP-S_PP-1);
177. end
178. else if (divide_count == M_PP+R_PP-S_PP-1)
179. begin
180.   if (~done_o) quotient <= quotient_node; // final shift...
181.   if (~done_o) quotient_reg <= quotient_node; // final shift (held output)
182.   done_o <= 1; // Indicate done, just sit
183. end
184. else // Division in progress
185. begin
186.   // If the subtraction yields a positive result, then store that result
```

Schematic /work/pwm_reader/pwm_reader

Layout - Magma Design Automation /work/pwm_reader/pwm_reader

Layout - Magma Design Automation /work/pwm_reader/pwm_reader

Layout - Magma Design Automation /work/pwm_reader/pwm_reader

Worst Case Analysis

and has a **hurtful 6ps** clock skew.

Cell Delay
Wire Delay

Data Path Delay

Cycle Adjust Slack

entity name	line	AT
89/pwm/rtl/verilog/serial_divide_uu.v	199	891
89/pwm/rtl/verilog/serial_divide_uu.v	199	892
89/pwm/rtl/verilog/serial_divide_uu.v	199	947
89/pwm/rtl/verilog/serial_divide_uu.v	199	949
89/pwm/rtl/verilog/serial_divide_uu.v	199	1017

NET: divider_unit.C589.IG12_2192_1

What EDA does not particularly well

- **Analog circuit synthesis**

- Same old Spice & layout with limited automation

- **Blocks of various shapes and sizes**

- Requires extensive manual tweaking

- **Speedup by parallel design algorithms**

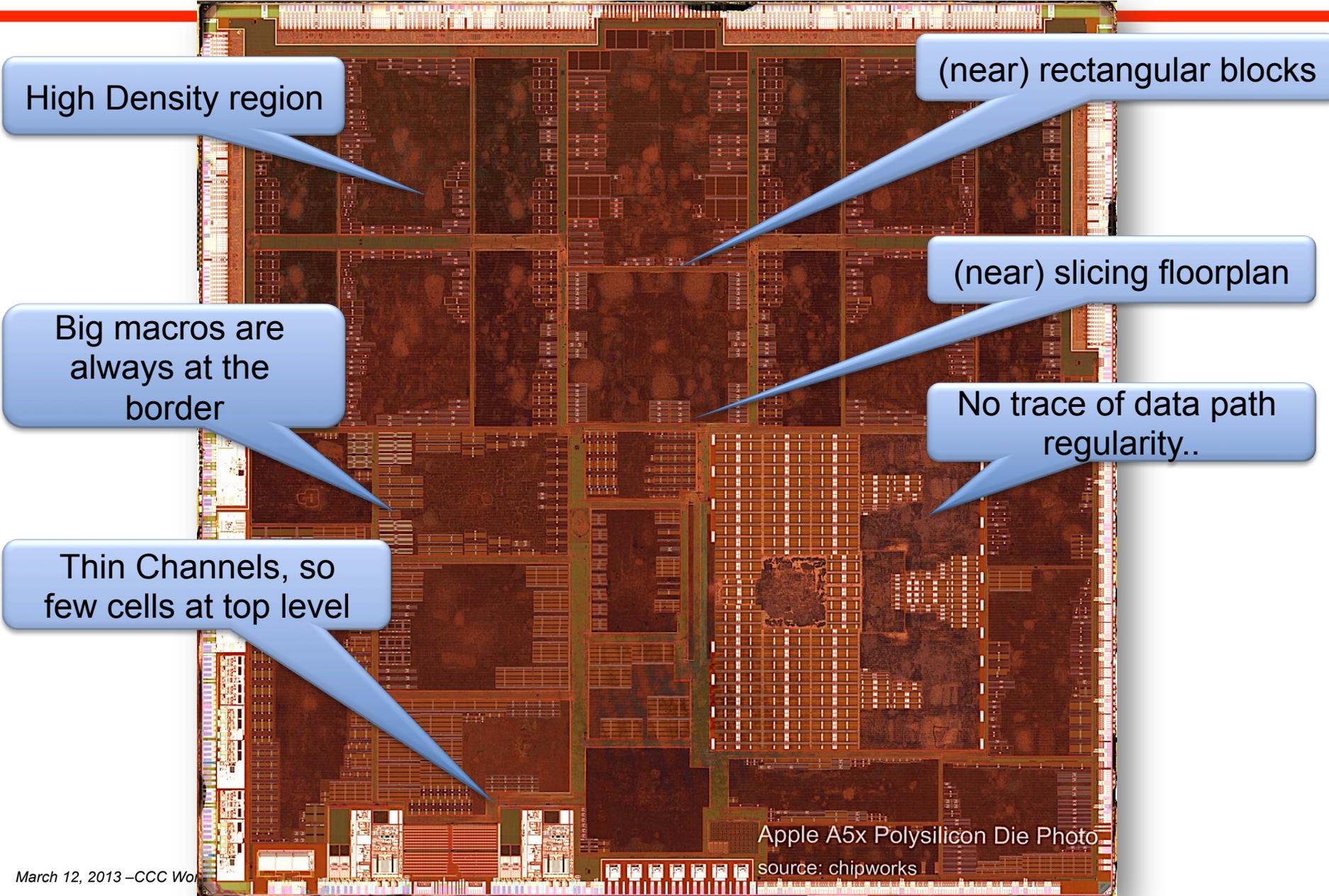
- Stuck at 4x

- **Higher levels of design abstraction**

- Gets domain-specific
- Many-objective flows

Hopeless
Hopeless
Hopeless
Must address

A closer look at the Apple's physical design style



High Density region

(near) rectangular blocks

Big macros are always at the border

(near) slicing floorplan

Thin Channels, so few cells at top level

No trace of data path regularity..

Apple A5x Polysilicon Die Photo
source: chipworks

“Many-Cell” Top-Level design

Magma Design Automation - Version 1.2.2c - Talus

File Viewers Window Help

layout_0

File View Select Add Edit Plan Pin Power Tools Help

Browse/Partition Hierarchy

More 'glue' at the top:
millions of cells

Hierarchy = evil
(but a necessary evil)

- Inverter ✓
- Buffer ✓
- Boolean ✓
- Complex ✓
- Latch ✓
- Flipflop ✓
- Tristate ✓
- Filler ✓
- Hyper cells
 - Hard Macro
 - Soft Macro
- Unbound cell: ✓
- Filter by Attrik
 - Position ✓
 - Keep ✓
- Access Point
- Blockage
- Power Synthesis

Layer Themes

Choose: Floorplan

Save Save As Delete

Depth Selection

View Depth: 100 Select Depth: 0

Show Basic Controls

Out ▲ In

◀ Full ▶

B15 ▼ F0

Drw ●

Point or drag to select. SHIFT to select multiple. CTRL to deselect.

x:11,886.225u y:192.240u Current Mode: Select Selected: 539867

Analysis(verification) tools: They were *not* the key to EDA success

- **Verification tools are overhyped. They are straightforward programming jobs:**
 - Use brute-force parallelism & cloud computing
 - Use tricks to keep memory usage low
 - Correlate to make result trustworthy
 - Use GPU if needed
- **Such tools exist in other domains as well:**
 - Mechanical CAD with finite element methods
 - Animation
 - Architecture

A few suggestions for good EDA research topics

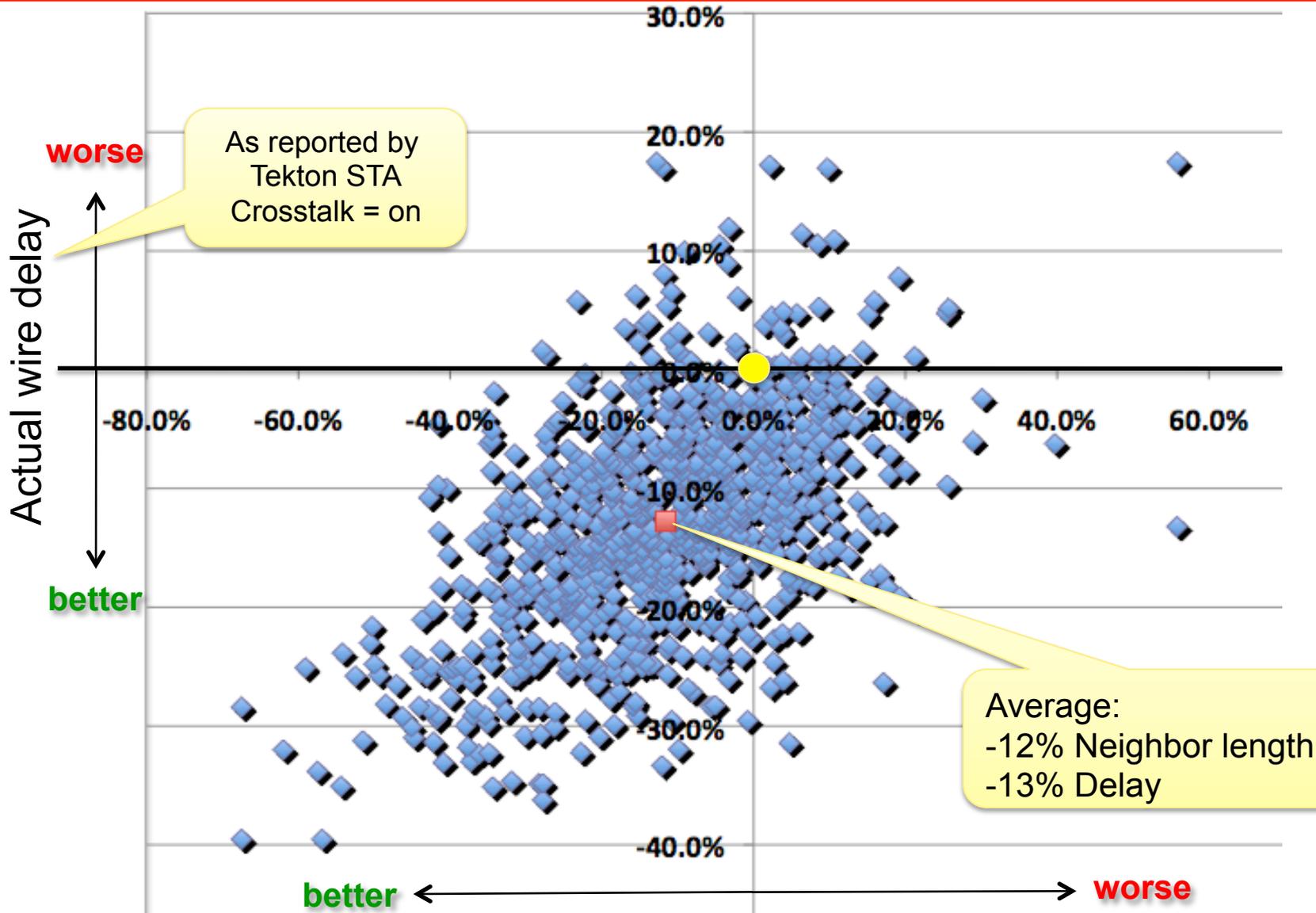
- **Better understanding the nature the beast:**
 - Bridging the Analysis – Implementation gap
 - Dealing with the noise of unreliable predictions
- **Radically new design paradigms**
 - Platforms, GALS/NoC
- **Radically new technologies**
- **Focus on ‘verticals’**
 - Automotive, mobile, aerospace, bio

Synthesis flow (or life) as a pachinko machine

- **Run complex flow:**
 - End up an one of the local optima.
- **Re-run:**
 - typically get same results
 - (Multi-processing alert!!)
- **Re-run with small change**
 - Could be huge difference
- **Changes:**
 - Irrelevant order changes
 - Additional steps/algorithms
 - Changing constraints, tuning, etc.



You always get what you want (not even close....)



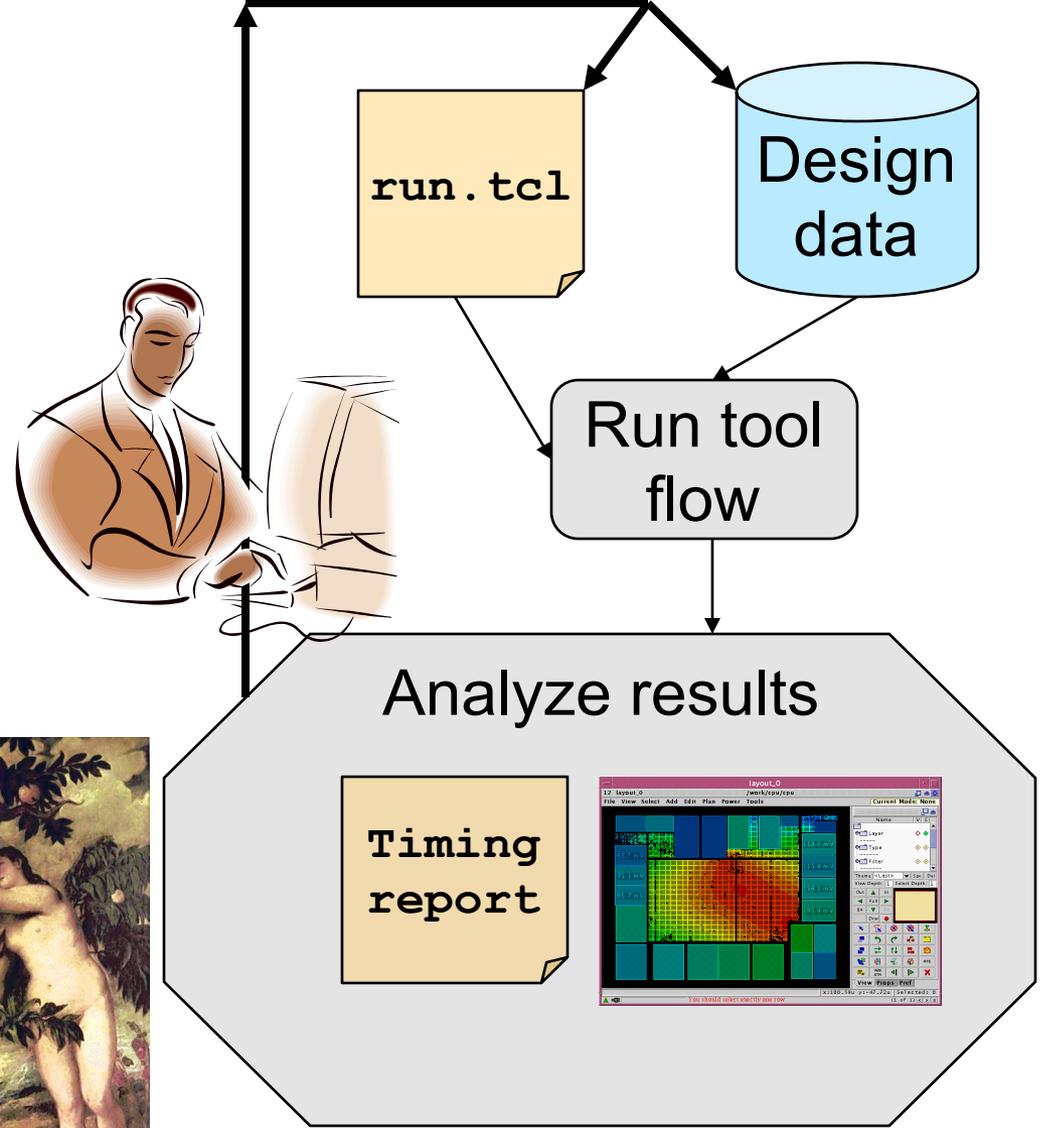
How to the better results from a noisy design system

- Run again and pray



- Run many times
 - Pick the best

- Attempt to understand
 - Cause, effect



Philosophical angle: Finding 'truth' in Engineering

- **With enough effort, its *always* possible to understand**
 - There are no miracles, only challenges to understand better
- **All decisions can be based on rational trade-offs on the best-available data:**
 - Effort vs quality
 - Power vs speed
 - Interest rate vs economic growth
 - CO2 output vs economic growth
 - Individual freedom vs taxes/abortion/
- **Shortcuts are necessary, because data is noisy/not understood**
 - But choices may not become dogma
- ***The great thing about science is it remains true whether you choose to believe it or not.***
 - Neil deGrasse Tyson

Using skeptical wisdom

- **“Humans are amazingly good at self-deception”**
 - This looks soooo good, therefore this *must* work
- **“If it has no side effects, it probably has no effects either”**
 - Example: improving temperature gradients is gonna cost you! So is improving yield. Are you really willing to pay based on the evidence?
- **“Do not confuse association with causation”**
 - “I took this airborne pill, and I did not get sick”
 - “I used this DFM optimizer, and the chip yields!”
- **“The plural of ‘anecdote’ is ‘anecdotes’, *not* data”**
 - Result could be a random effect, or another side effect
 - No substitute for unbiased placebo-controlled tests
 - Only large data sets are statistically relevant

Summary

- **EDA is maturing, but far from solved!**
 - Main issue: keeping up with Moore's law
- **Academia has unique chance to set research direction for EDA**
- **Advice:**
 - Less algorithms, more methodologies
 - EDA requires a 'holistic' methodology across many abstraction levels
 - ...rather than 'optimal' point tool solutions
 - Resist temptation to do too much short-term development work
 - Focus on big problems that matter:
 - Paradigms to deal with design scale
 - Understanding and controlling complex flows
- **Best way: Start a new company yourself**