EDA at the End of Moore's Law

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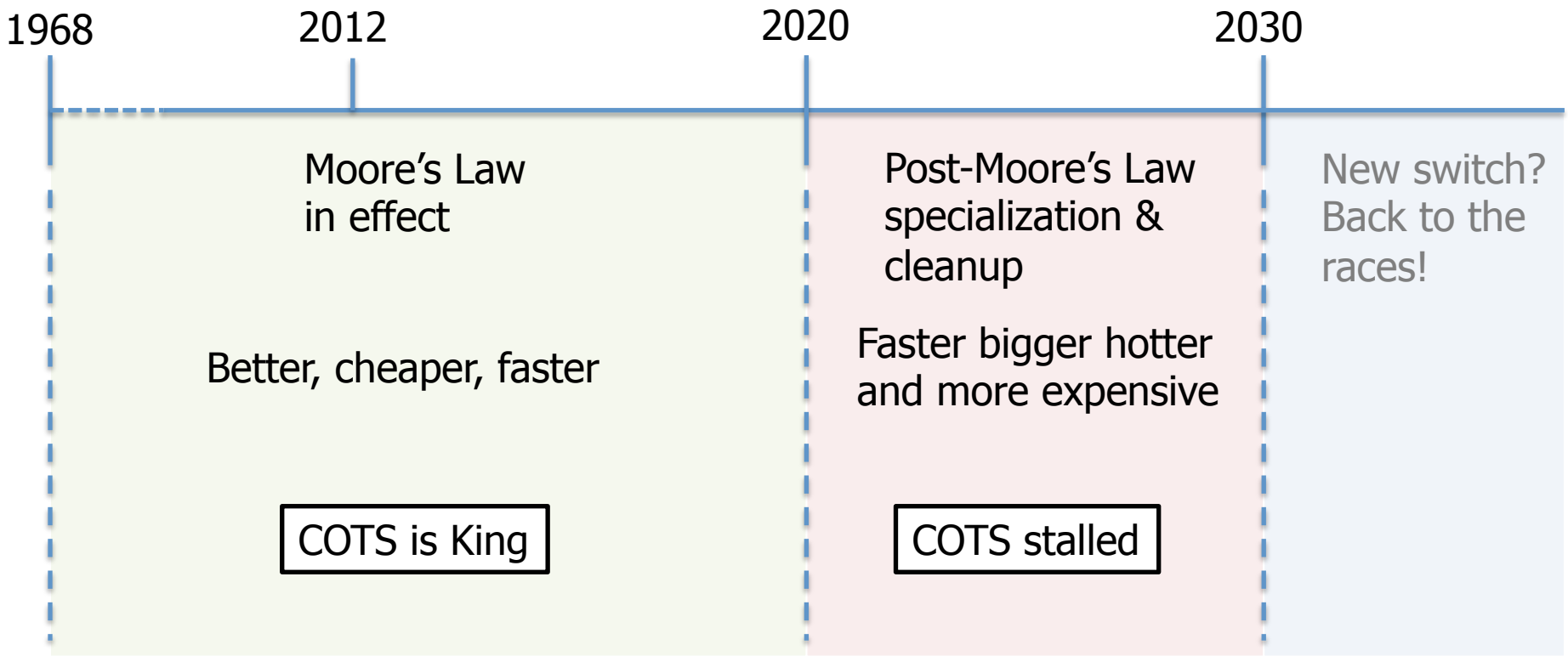
This talk…

This is a Dept of Defense–centric view of the overall CAD universe

1. First let's talk about Moore's Law (and its impending demise)
2. Then we'll talk about the implications for EDA

My model: During and After Moore's Law

1. COTS is both problem & opportunity for DoD for next 10 years.
2. Then COTS stalls out. (But DoD doesn't have to!)

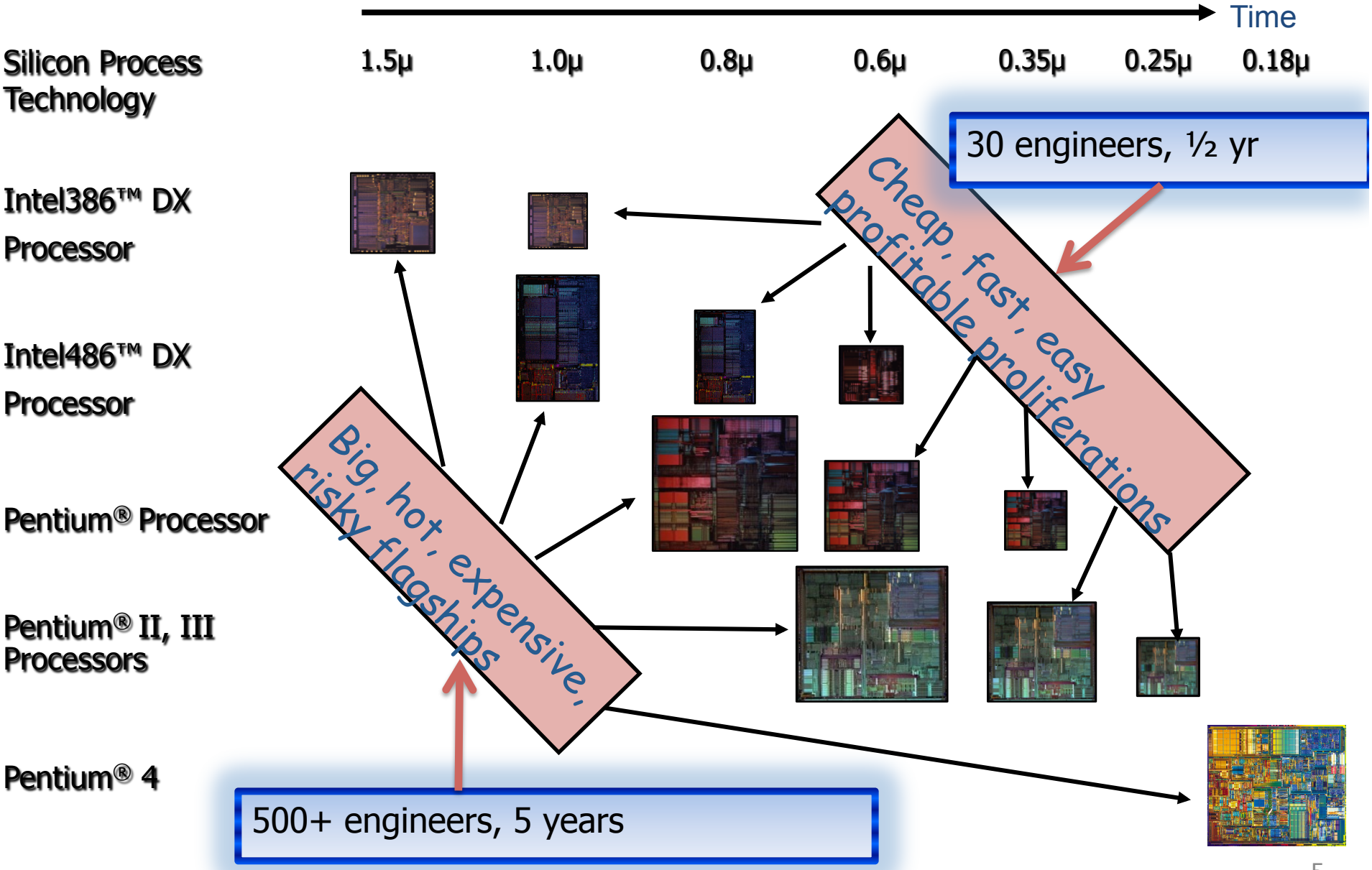


…and then what? What About After Moore's Law Ends?

Some observations:

- COTS improvements will slow to a trickle within 10 years
  - Not a question of if, but when
- There were electronics and computer advances before Moore's Law, and there will be some after it
  - But they will be small and relatively infrequent, no longer routine
  - Software still has several years of runway before stalling
- Economics will likely die first, when incremental products are no longer valued by paying customers
  - Even though physics & fab challenges are already dire
- Effect: you can no longer just wait and get faster chips
  - This will boost motivation for specialized engines (1000x left on table)
- Let's talk more about Moore's Law…

Classic Moore's Law: Made New Designs Possible, Old Ones Lucrative



It Was a Great Ride, But It's Ending

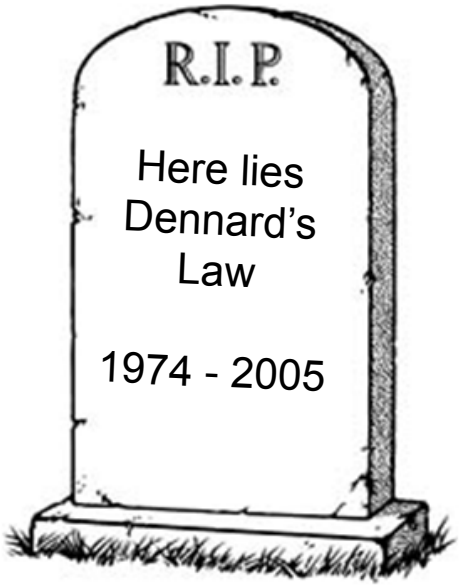
Moore's Law put lots more transistors on a chip…

…but it's Dennard's Law that made them useful

Dennard's Law has been repealed.

Moore's Law: 2x transistors every 2 years

Dennard's Law: transistors will be faster and lower energy



2011 NRC/CSTB Study: "The Future of Computing Performance"

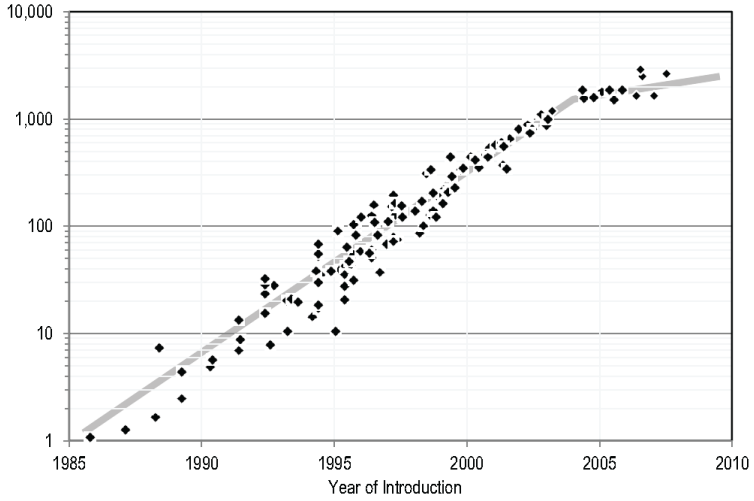


FIGURE A.1 Integer application performance (SPECint2000) over time (1985-2010).

Clock freq stalled, because

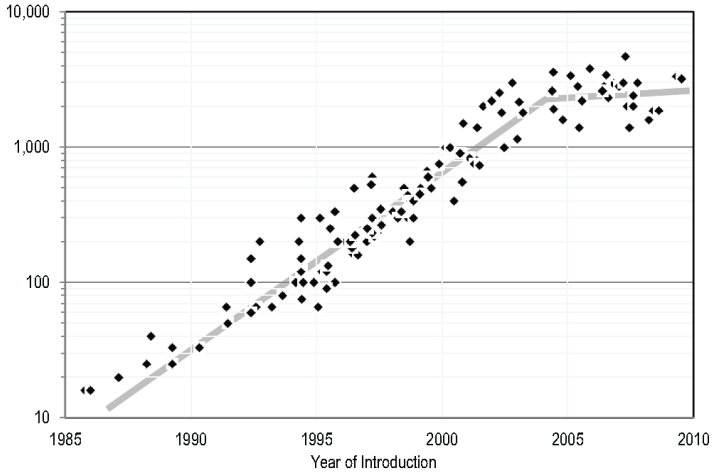


FIGURE A.3 Microprocessor clock frequency (MHz) over time (1985-2010).

Single-threaded perf stalled, because

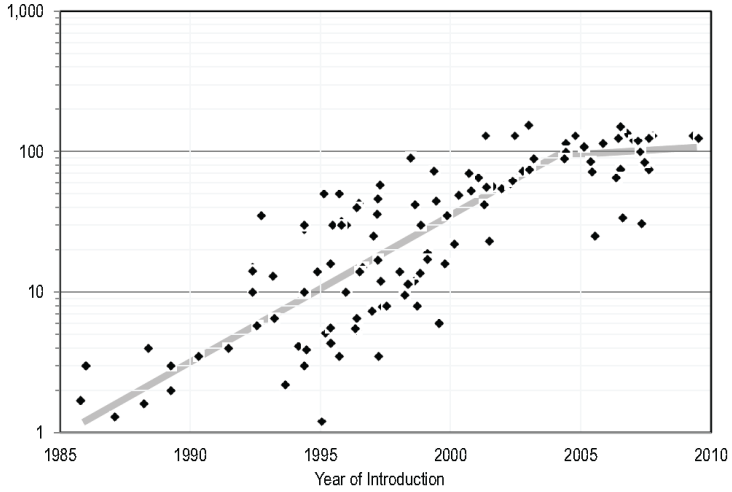
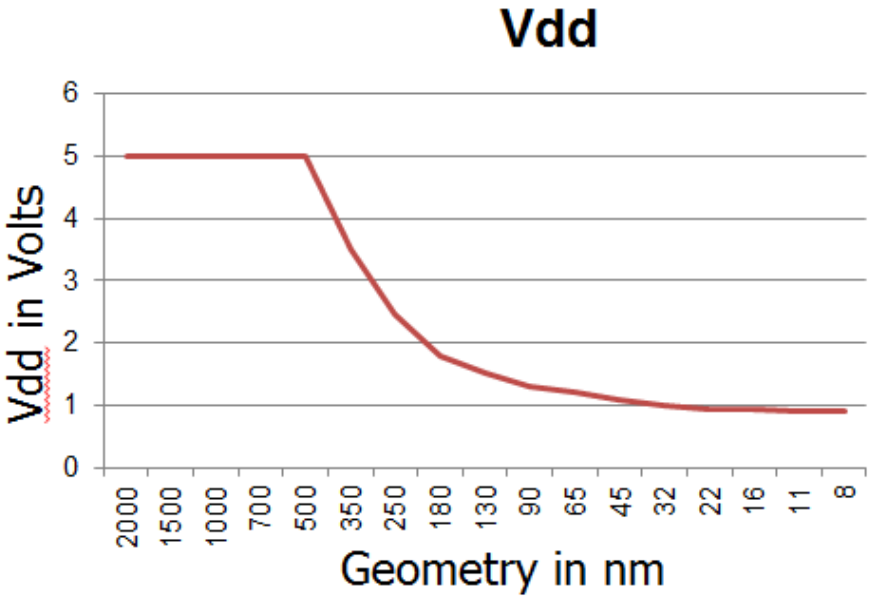


FIGURE A.4 Microprocessor power dissipation (watts) over time (1985-2010).

Power hit a cooling wall.

Why did we hit a power/cooling wall?



Data courtesy S. Borkar/Intel 2011

- Voltage scaling slowed drastically
- Asymptotically approaching threshold

$$P = N_g C_{load} f V^2$$

N_g = CMOS gates/unit area
C_{load} = capacitive load/CMOS gate
f = clock frequency
V = supply voltage

The good old days of Dennard Scaling:

$$P_{density} = (k^2)(\tfrac{1}{k})(k)(\tfrac{1}{k^2}) = 1$$

Today, now that Dennard Scaling is dead:

$$P_{density} = (k^2)(\tfrac{1}{k})(k)(\tfrac{1}{k^2}) = k^2$$

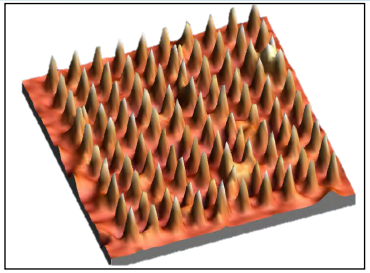
Typical $k = 1.4$, so $k^2 \cong \mathbf{2}$

Remaining Avenues for Improvements

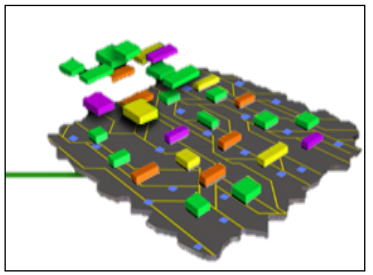
1. Near term: specialized processing (e.g., graph processors, GPUs)
2. Heterogeneous parallelism (dedicated HW)
3. Fix resulting resiliency issues (using both HW & SW)
4. Better cooling methods (boost cooling efficiency, spend on perf)
5. Better algorithms, tools, simulations, emulations
6. **Drive costs, time-to-market down**
7. **Hope industry & academia come up with replacement switch technology in time!**

Some Current DARPA/MTO Programs

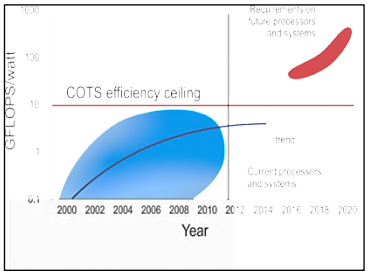
Probabilistic designs: UPSIDE



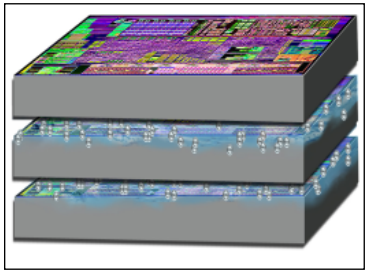
3D die stacking: DAHI



Huge heterogeneous fabrics: PERFECT



New Cooling Techniques: ICECool



I Think Moore's Law is Indirectly to Blame for SW Costs

- Moore's Law has enabled very high-level languages, tremendous capabilities/ features (executable sizes, processor speeds)
- Bad: Design complexity migrates to system point of least resistance: SOFTWARE
- How can EDA help project leaders say NO when they need to?
  - Much more compelling to point to tools as evidence, than gut instinct
  - Can't automate necessary human judgment (e.g. project risk) but can provide quantitative data to inform that judgment

LAW NUMBER XVI

In the year 2054, the entire defense budget will purchase just one aircraft. This aircraft will have to be shared by the Air Force and Navy 3 days each per week except for leap year, when it will be made available to the Marines for the extra day.

Norm Augustine, "Augustine's Laws"

But the "gorilla in the room," General Bogdan said, is testing and securing the 24 million lines of software code for the plane and its support systems, a mountain of instructions that goes far beyond what has been tried in any plane.

And writing and testing the millions of lines of software needed by the jets is so daunting that General Bogdan said, "It scares the heck out of me."

NY Times Nov. 29, 2012

EDA Challenges at the end of Moore's Law

1. Simulations will have to include both HW and SW

   Where SW means {application, runtime, OS}

2. Simulations will have to model much more than just function (for V&V)

   Performance across huge numbers of hetero cores (each with own voltage regulator), Power delivery and dissipation, resilience management in HW and SW, photonics and electronics intermixed, 3D stacking, NTV circuits, quantitative system resilience prediction, data locality effects, packaging…ALL AT DESIGN TIME

3. EDA Business Economics will have to work

   Opposing forces:

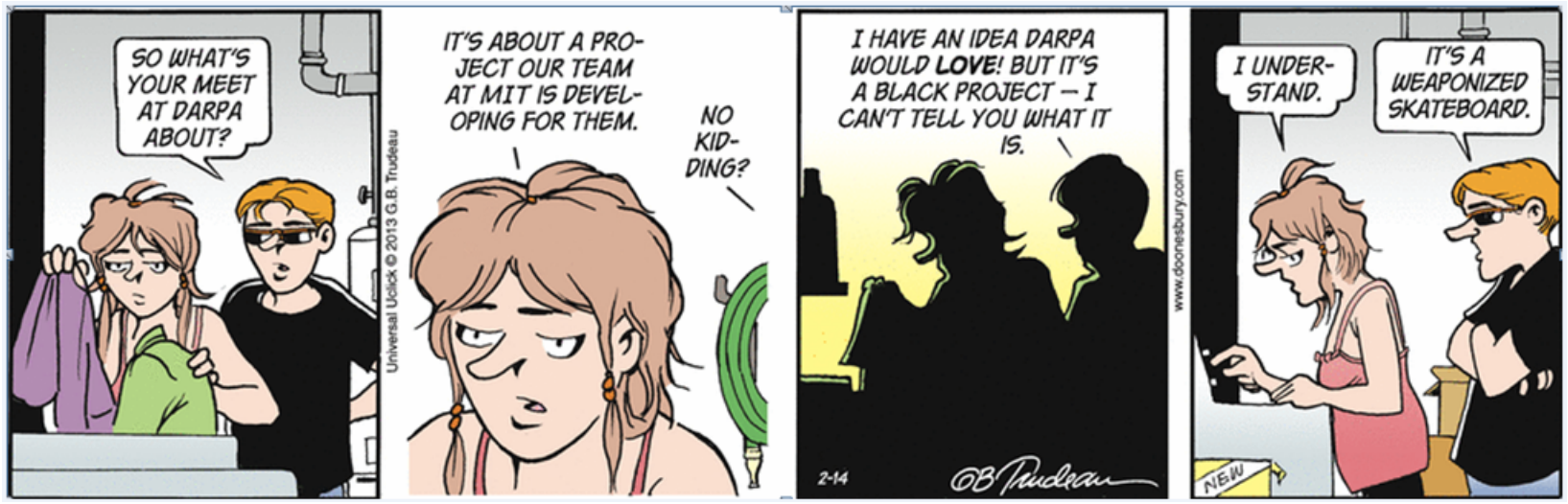
☹ Extremely high mask set costs, extremely high chip functional density and complexity, will discourage new custom or ASIC designs, lowering demand for EDA tools

☺ End of Moore's Law will open a window for specialized silicon that will no longer be in danger from a COTS processor 2 years down the road

4. Watch for scale

EDA solution for exascale may be very inappropriate for what most designers need in 2025

Q & A



www.darpa.mil